

ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005 1.1 GHz Super Low Power **Dual Modulus Prescaler**

The MC12052A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7 mW at a minimum supply voltage of 2.7 V.

The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0 mA Typical
- 2.0 mA Maximum, −40 to 85°C, V_{CC} = 2.7 to 5.5 Vdc
- Short Setup Time (t_{Set}) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola

FUNCTIONAL TABLE

sw	MC	Divide Ratio
Н	Н	64
Н	L	65
L	Н	128
L	L	129

NOTES: 1. SW: H = V_{CC}, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.

2. MC: H = 2.0 V to V_{CC} , L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	VCC	-0.5 to 7.0	Vdc
Operating Temperature Range	TA	-40 to 85	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C
Modulus Control Input, Pin 6	МС	-0.5 to 6.5	Vdc

MC12052A

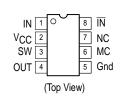
MECL PLL COMPONENTS ÷64/65, ÷128/129 LOW POWER **DUAL MODULUS PRESCALER**

SEMICONDUCTOR **TECHNICAL DATA**



D SUFFIX PLASTIC PACKAGE **CASE 751** (SO-8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temp Range	Package	
MC12052AD	T _A =-40 to 85°C	SO-8	

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ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5 VDC, T_A = -40 to 85°C, unless otherwise noted.)

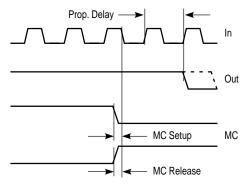
,					
Characteristic	Symbol	Min	Тур	Max	Unit
A Roggill Viequency (Sine Wave Cinput) ESEMICONDUCTOR,	NC. 2005	0.1	1.4	1.1	GHz
Supply Current (Pin 2)	ICC	_	1.0	2.0	mA
Modulus Control Input High (MC)	V _{IH1}	2.0	-	V _{CC} + 0.5 V	V
Modulus Control Input Low (MC)	V _{IL1}	Gnd	-	0.8	V
Divide Ratio Control Input High (SW)	V _{IH2}	V _{CC} – 0.5 V	VCC	V _{CC} + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V _{IL2}	Open	Open	Open	1
Output Voltage Swing (Note 2) ($C_L = 8.0 \text{ pF}, R_L = 3.3 \text{ k}\Omega$)	V _{out}	0.8	1.1	_	VPP
Modulus Setup Time MC to Out @ 1100 MHz	t _{set}	-	11	16	ns
Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	V _{in}	100 400	- -	1000 1000	mV _{PP}
Output Current (Note 1) $ \begin{array}{c} \text{V}_{CC} = 2.7 \text{ V, } C_L = 8.0 \text{ pF, } R_L = 3.3 \text{ k}\Omega \\ \text{V}_{CC} = 5.0 \text{ V, } C_L = 8.0 \text{ pF, } R_L = 7.2 \text{ k}\Omega \end{array} $	IO	<u>-</u>	0.5 0.5	3.0 3.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 1.1 GHz

Figure 1. Logic Diagram (MC12052A)

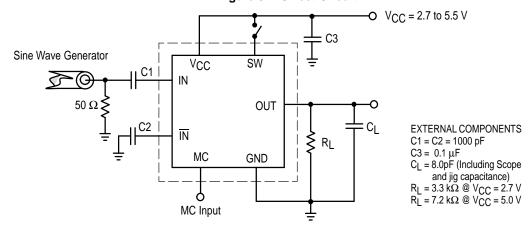
В QB QB D Q QB QE D QB D Е G Н QB QB SW-

Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 3. AC Test Circuit

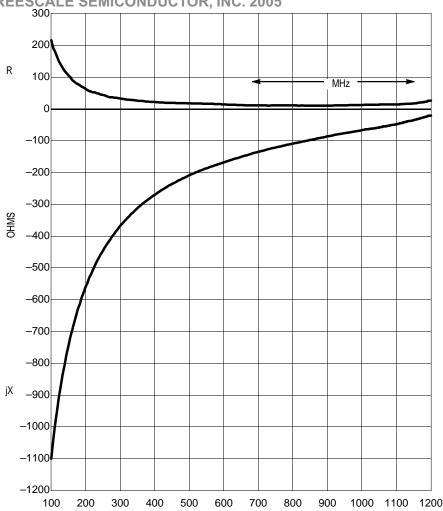


^{2.} Valid over voltage range 2.7 to 5.5 V; R_L = 3.3 k Ω @ V_{CC} = 2.7 V; R_L = 7.2 k Ω @ V_{CC} = 5.0 V

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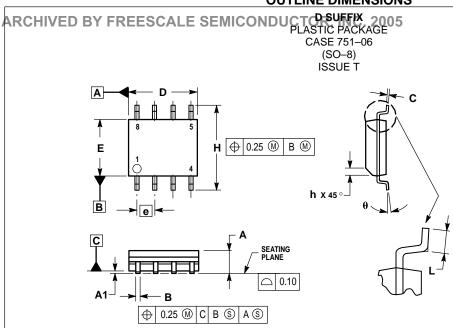
Figure 4. Typical Input Impedance versus Input Frequency

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OUTLINE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. DIMENSIONS ARE IN MILLIMETER.
- DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS			
DIM	MIN	MAX		
Α	1.35	1.75		
A1	0.10	0.25		
В	0.35	0.49		
С	0.19	0.25		
D	4.80	5.00		
Е	3.80	4.00		
е	1.27	1.27 BSC		
Н	5.80	6.20		
h	0.25	0.50		
L	0.40	1.25		
θ	0°	7°		

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